CLAIMS

1. A PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising:

a current detecting circuit for detecting a current value of an output current; and

a controller for outputting a zero vector to be started from an O state in which all phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value measured by the current detecting circuit is equal to or greater than a first reference value which is preset and has a lower level than a level of a second reference value which is higher than a level of the first reference value, carrying out a base block operation for bringing all of the switching units into an OFF state after outputting the zero vector when the current value is equal to or greater than the second reference value and has a lower level than a level of a third reference value which is higher than the level of the second reference value, and executing an emergency stop when the current value is equal to or greater than the third reference value.

2. The PWM inverter control apparatus according to claim 1, wherein the controller carries out a reset to a normal operation after performing a zero vector output operation when executing the reset to the normal operation after carrying out the base block operation.

3. A PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising:

a current detecting circuit for detecting a current value

of an output current; and

a controller for outputting such a zero vector as to bring an O state in which all of phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage and then carrying out a base block operation for bringing all of the switching units into an OFF state when the current value measured by the current detecting circuit is equal to or greater than a preset reference value, and for outputting such a zero vector as to bring all of the phases into the O state and then performing a reset to a normal run when the current value is smaller than the reference value.

4. The PWM inverter control apparatus according to any of claims 1 to 3, wherein the zero vector is started from an OOO state in which all of the phases are turned ON by the second and third switching units from the DC bus voltage side having the plus level to output the intermediate potential to be the voltage between the plus and minus levels of the DC bus voltage, and

the zero vector is always brought into the OOO state between a PPP state in which all of the phases are turned ON by first and second switching units from the DC bus voltage side having the plus level to output the plus level of the DC bus voltage and an NNN state in which all of the phases are turned ON by third and fourth switching units from the DC bus voltage side having the plus level to output the minus level of the DC bus voltage.

5. A PWM inverter control method for controlling a PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising the steps of:

detecting a current value of an output current;

outputting a zero vector to be started from an O state in which all phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value is equal to or greater than a first reference value which is preset and has a lower level than a level of a second reference value which is higher than a level of the first reference value;

carrying out a base block operation for bringing all of the switching units into an OFF state after outputting the zero vector when the current value is equal to or greater than the second reference value and has a lower level than a level of a third reference value which is higher than the level of the second reference value; and

executing an emergency stop when the current value is equal to or greater than the third reference value.

6. The PWM inverter control method according to claim 5, further comprising a step of carrying out a reset to a normal operation after performing a zero vector output operation when executing the reset to the normal operation after carrying out the base block operation.

7. A PWM inverter control method for controlling a PWM inverter control apparatus in which four switching units are connected in series for each phase between a DC bus voltage having a plus level and a DC bus voltage having a minus level, comprising the steps of:

detecting a current value of an output current;

outputting such a zero vector as to bring an O state in which all of phases are turned ON by second and third switching units from the DC bus voltage side having the plus level to output an intermediate potential to be a voltage between the plus and minus levels of the DC bus voltage when the current value is equal to or greater than a preset reference value;

carrying out a base block operation for bringing all of

the switching units into an OFF state after outputting the zero vector; and

outputting such a zero vector as to bring all of the phases into the O state and then performing a reset to a normal run when the current value is smaller than the reference value.

8. The PWM inverter control method according to any of claims 5 to 7, wherein the zero vector is started from an OOO state in which all of the phases are turned ON by the second and third switching units from the DC bus voltage side having the plus level to output the intermediate potential to be the voltage between the plus and minus levels of the DC bus voltage, and

the zero vector is always brought into the OOO state between a PPP state in which all of the phases are turned ON by first and second switching units from the DC bus voltage side having the plus level to output the plus level of the DC bus voltage and an NNN state in which all of the phases are turned ON by third and fourth switching units from the DC bus voltage side having the plus level to output the minus level of the DC bus voltage.